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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3 November 2008 have been fully considered but they are not persuasive.

2. Applicant traverses the 35 USC 103(a) rejection of claim 19 as being unpatentable over US Patent No. 6,731,335 issued to Kim et al., (hereinafter "Kim") in view of US Patent No. 6,522,357 issued to Beiley arguing that:

(1) Beiley does not disclose a shutter transistor and storage node, wherein the shutter transistor is connected to and transferring charge from a respective photosensor to a respective storage node and therefore does not teach that "an electronic shutter can be achieved in a CMOS image sensor by using a shutter transistor and a storage node";

(2) Applicant's invention, as exemplified by Figure 3, enables (1) the floating diffusion region [to] be reset at the same time the image is captured and (2) increas[ing] the capacity of the storage node.

3. Regarding Applicant's first argument, Beiley *explicitly* discloses a shutter transistor (Figure 1, "pass transistor M2") connected to and transferring charge from a respective photosensor (Figure 1, "14") to a respective storage node (Figure 1, "node 2"). Further, Beiley *explicitly* discloses that "[t]he present invention relates generally to CMOS image sensors and particularly to a method and apparatus for increasing retention time in image sensors having an electronic shutter". Therefore, Beiley

discloses that "an electronic shutter can be achieved in a CMOS image sensor by using a shutter transistor and a storage node".

As stated in the Final Office Action dated 2 July 2008, the Examiner relies on Kim to disclose that plural photodiodes can share a reset transistor, a drive transistor and a select transistor in a CMOS image sensor. Beiley is relied on to teach that an electronic shutter can be achieved in a CMOS image sensor by using a shutter transistor and a storage node. A person having ordinary skill in the art of CMOS image sensors would realize that an electronic shutter could be achieved in the image sensor disclosed by Kim via a shutter transistor and a storage node for each photodiode as disclosed by Beiley. Therefore, supplementing the teachings of Kim with Beiley achieve the required limitations of claim 19. As stated in non-final Office Action dated 31 December 2007, one would have motivation to do so in order to avoid using a mechanical shutter. Stated another way, the Examiner contends that a person having ordinary skill in the art of CMOS image sensors would realize that taking “transistor M2” and “storage node 2” of Beiley, Figure 1 and adding this configuration to Figure 4 of Kim (i.e. one transistor and storage node for each photodiode) is obvious in order to achieve an electronic shutter in the invention disclosed by Kim. Further, one would have motivation to do so in order to avoid using a mechanical shutter.

4. Regarding Applicant’s second argument, it is noted that the features upon which applicant relies (i.e., (1) the floating diffusion region [to] be reset at the same time the image is captured and (2) increas[ing] the capacity of the storage node) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification,

limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Further, please note that Kim discloses that the floating diffusion region is reset at the same time the image is captured (refer to the timing chart of Figure 5, Rx is on (i.e. reset is occurs) while the photodiodes integrate ("B1", c. 5, ll. 34-40 and "B2", c. 5, ll. 47-53)).

5. For these reasons, the previous rejection is maintained.

/David L. Ometz/

Supervisory Patent Examiner, Art Unit 2622